<u>The Invention Claimed Is</u>

1. A variable delay cell comprising:

a plurality of load resistance transistors connectable in parallel with one another;

a plurality of bias current transistors connectable in parallel with one another;

a switching transistor connected in series between the plurality of load resistance transistors and the plurality of bias current transistors; and

switching circuitry configured to selectively operatively connect at least one of the load resistance transistors in parallel with at least one other of the load resistance transistors.

2. The variable delay cell defined in claim 1 further comprising:

further switching circuitry configured to selectively operatively connect at least one of the bias current transistors in parallel with at least one other of the bias current transistors.

3. The variable delay cell defined in claim 1 further comprising:

a plurality of further load resistance transistors connectable in parallel with one another; and

a further switching transistor connected in series between the plurality of further load resistance transistors and the plurality of bias current transistors, wherein the switching transistor and the further switching transistor are respectively controlled by complementary input signals.

4. The variable delay cell defined in claim 3 wherein the switching circuitry is further configured to selectively operatively connect at least one of the further load resistance transistors in parallel with at least one other of the further load resistance transistors.

5. The variable delay cell defined in claim 1 wherein the switching circuitry is programmable.

6. The variable delay cell defined in claim 2 wherein the further switching circuitry is programmable.

7. The variable delay cell defined in claim 1 wherein the switching circuitry is configured to selectively apply either a disabling control signal or a variable control signal to the at least one of the load resistance transistors.

8. The variable delay cell defined in claim 7 wherein the variable control signal is also used to control the at least one other of the load resistance transistors.

9. The variable delay cell defined in claim 7 wherein the further switching circuitry is configured to selectively apply either a deactivating control signal or a variable activating control signal to the at least one of the bias current transistors.

10. The variable delay cell defined in claim 9 wherein the variable activating control signal is also used to control the at least one other of the bias current transistors.

11. A programmable delay cell comprising:

a plurality of load resistance transistors connected in parallel with one another;

a plurality of bias current transistors connected in parallel with one another;

a switching transistor connected in series between the plurality of load resistance transistors and the plurality of bias current transistors; and

switching circuitry configured to selectively apply either a substantially fixed deactivating control signal or a variable activating control signal to at least one of the load resistance transistors.

12. The programmable delay cell defined in claim 11 further comprising:

control circuitry configured to apply the variable activating control signal to at least another one of the load resistance transistors.

13. The programmable delay cell defined in claim 11 further comprising:

further switching circuitry configured to selectively apply either a substantially fixed disabling control signal or a variable enabling control signal to at least one of the bias current transistors.

14. The programmable delay cell defined in claim 13 further comprising:

further control circuitry configured to apply the variable enabling control signal to at least another one of the bias current transistors.

15. The programmable delay cell defined in claim 11 further comprising:

a plurality of further load resistance transistors connected in parallel with one another; and

a further switching transistor connected in series between the plurality of further load resistance transistors and the plurality of bias current transistors, wherein the switching transistor and the further switching transistor are respectively controlled by complementary input signals.

16. The programmable delay cell defined in claim 15 wherein the switching circuitry is further configured to selectively apply either the substantially fixed deactivating control signal or the variable activating control signal to at least one of the further load resistance transistors.

17. A programmable differential delay cell comprising:

a plurality of first load resistance transistors connected in parallel with one another;

a plurality of second load resistance transistors connected in parallel with one another;

a plurality of bias current transistors connected in parallel with one another;

a first switching transistor connected in series between the plurality of first load resistance transistors and the plurality of bias current transistors;

a second switching transistor connected in series between the plurality of second load resistance transistors and the plurality of bias current transistors;

input circuitry configured to respectively apply first and second differential input signals as control signals to the first and second switching transistors;

first switching circuitry configured to selectively activate at least one of each of the first and second load resistance transistors for operation in parallel with at least one other of the first and second load resistance transistors, respectively; and

second switching circuitry configured to selectively activate at least one of the bias current transistors for operation in parallel with at least one other of the bias current transistors.

18. The programmable differential delay cell defined in claim 17 further comprising:

output circuitry configured to respectively derive first and second differential output signals from electricity flow controlled by the first and second switching transistors.

19. Voltage controlled oscillator circuitry comprising:

a plurality of programmable differential delay cells as defined in claim 18 connected in a

closed loop series in which the input signals of each cell are the output signals of a preceding cell in the series.

20. Phase locked loop circuitry comprising:

voltage controlled oscillator circuitry as defined in claim 19; and

phase/frequency detector circuitry configured to compare phase and frequency of a signal in the voltage controlled oscillator circuitry to phase and frequency of a time-varying input signal in order to produce output control signals for at least partly controlling the first and second load resistance transistors and the bias current transistors.

21. A programmable logic device comprising:

phase locked loop circuitry as defined in claim 20.

22. The programmable logic device defined in claim 21 further comprising:

programmable logic circuitry configured to make use of a signal produced as a result of operation of the phase locked loop circuitry.

23. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

a programmable logic device as defined in claim 22 coupled to the processing circuitry and the memory.

24. A printed circuit board on which is mounted a programmable logic device as defined in claim 22.

25. The printed circuit board defined in claim 24 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic device.

26. The printed circuit board defined in claim 24 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable logic device.